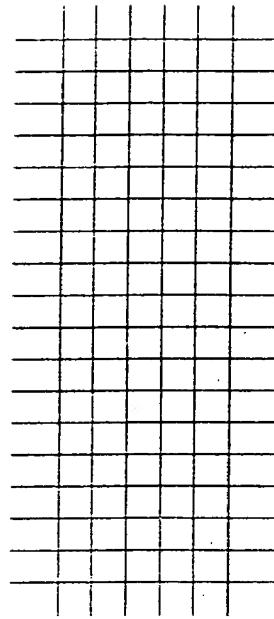




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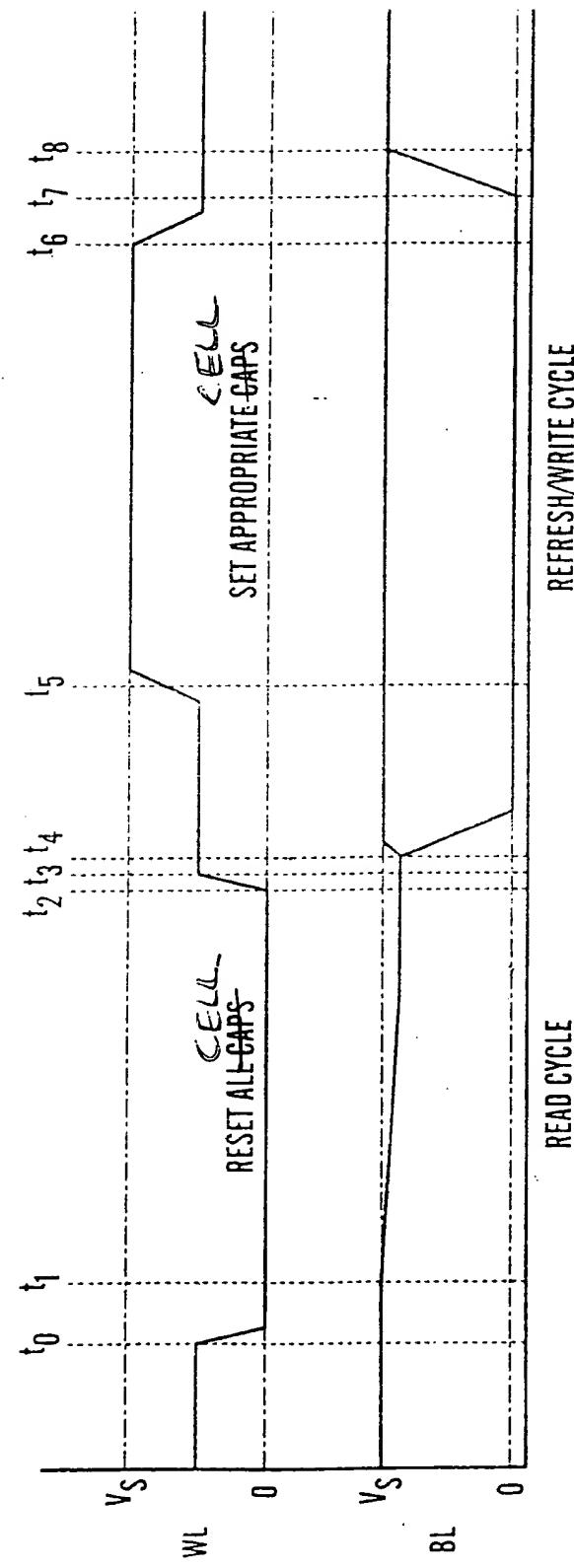
- t_0 : WORD LINE LATCHED, ACTIVE PULLDOWN TO 0
- t_1 : BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2 : BIT LINE DECISION - DATA LATCHED
- t_3 : WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_4 : WRITE DATA LATCHED ON BIT LINES
- t_5 : WORD LINE PULLED TO V_s - SET/RESET SENSE AMPS CELL
- t_6 : WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_7 : BIT LINES ACTIVELY RETURNED TO V_s CLAMP
- t_8 : READ/WRITE CYCLE COMPLETE

MAXIMUM DEPOLARIZING VOLTAGE $V_s/2$



WORD LINES AT $V_s/2$

SENSE AMPS BIASED NEAR V_s



REFRESH/ WRITE CYCLE

READ CYCLE

Fig. 4



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